IN THE SPECIFICATION:

Please amend the first full paragraph appearing on page 2 as follows:

Field of the Invention: The present invention relates generally to the use of a ~~non-volatile~~ non-volatile storage device, such as an electrically erasable programmable read only memory device ("EEPROM"), to store information regarding the location of failed parts on a multi-chip module such as a memory module. More particularly, the present invention relates to storing, in an on-module EEPROM, the identities of module output terminals, such as data query ("DQ") terminals which, during testing of the module, have been determined to fail and are thus indicative of the locations of corresponding failed components.

Please amend the second full paragraph appearing on page 2 as follows:

State of the Art: Recent computer memory modules include a non-volatile storage device, such as an electrically erasable programmable read only memory device ("EEPROM"), an erasable programmable read only memory device ("EPROM"), a ~~ferro-electronic~~ ferro-electronic device or a flash memory chip, on the memory module with other volatile storage devices such as random access memory ("RAM"), synchronous dynamic random access memory ("SDRAM") and dynamic random access memory ("DRAM"). Volatile storage devices are those memory devices in which information stored in a memory cell in the device is completely lost when the power supply voltage applied to the memory cell is interrupted or turned off. In contrast, information stored in the cells of non-volatile storage devices is preserved when the power supply is turned off. A non-volatile storage device on a memory module is conventionally used to store valuable configuration information necessary for the processor to access the memory on the module. The configuration information stored on the non-volatile storage device includes such parameters as the latency and speed of the module components and the size and type of memory module, ~~and are~~ and is accessed by the processor during initialization of the system. The memory of the EEPROM is divided into sections, each section storing a different category of information.

Please amend the first full paragraph appearing on page 3 as follows:

Typically, however, the capacity of the EEPROM, or other long-term memory storage device, is greater than the memory requirements for the configuration information ~~which~~ that needs to be stored. The industry has established a standard of a minimum of 128 bytes as the volume of configuration data to be stored on the non-volatile storage device. Therefore, any EEPROM memory (in excess of 128 bytes) remaining unused may be used to store additional information that is not material to the functionality of the module. The memory capacity of an EEPROM in excess of 128 bytes varies by the capacity of the EEPROM used.

Please amend the paragraph bridging pages 3 and 4 as follows:

U.S. Patent 5,996,096 to Dell et al. (November 30, 1999), the disclosure of which is hereby incorporated herein by reference, discloses using the excess memory capacity of an EPROM mounted on a memory module to store a map of the bad memory addresses of "reduced specification DRAM chips" ~~(e.g.~~ (e.g., chips with nonfunctional memory addresses or partially defective DRAM chips) for use during operation of the memory module. According to the invention of Dell et al., each of a plurality of memory chips or dice is coded and marked with a unique identifier and tested in accordance with conventional testing methods. ~~Figures~~ FIGS. 1-3 depict an example of the invention of Dell et al. using a 72 pin single in-line memory module ("SIMM") 2 comprising a printed circuit board ("PCB") 4 having a plurality of electrical contacts 6 (72 in the illustrated example) along one edge. Those tested memory chips having one or more bad memory cells are identified as "reduced specification chips" 8, 10, 12, 14, 16, 18, 20 and 22 and are placed together on the SIMM 2. The reduced specification chips are identified and their positions recorded using their respective unique identifiers (not shown). The address maps which identify specific bad addresses for each of the chips 8, 10, 12, 14, 16, 18, 20 and 22 are programmed into an EPROM 24 placed on the PCB 4 and associated with each of the respective unique identifiers of the chips 8, 10, 12, 14, 16, 18, 20 and 22. During later testing or operation of the memory module, the address map stored in the EPROM 24 is routinely accessed and updated by system processes to enable a logic device 26, such as an ~~application specific~~ application-specific integrated circuit ~~("ASIC"),~~ ("ASIC") or other programmable logic device

~~which~~ that contains the bit steering logic and timing generation logic, to redirect the data for defective DRAM addresses to an alternate storage device for all read and write operations in real time.

Please amend the third full paragraph appearing on page 4 as follows

Memory chip manufacturers conventionally employ ~~chip testing~~ chip-testing systems to individually test each memory chip. These systems test the operability of each memory chip by writing a value into each memory cell within the chip and then reading the contents of that cell. An example of an individual chip testing system is described in U.S. Patent 5,991,215 to Brunelle (Nov. 23, 1999), the disclosure of which is hereby incorporated herein by reference.

Please amend the second full paragraph appearing on page 5 as follows:

To illustrate how the testing process may affect the cost of a memory module, consider the following example. A process ~~which could~~ that can test 16 memory modules in parallel through a ~~5 minute~~ five-minute test would produce 192 modules per hour. Assuming a 25% failure rate, which is not atypical, there would be 48 of the 192 memory modules tested ~~which~~ that fail the test process. However, when testing 16 modules at a time in parallel, identifying and marking failures by watching a test monitor during testing is no longer feasible. The modules identified as failed are therefore retested, one at a time, to identify which parts failed for each module. Due to parallelism, the time it takes to test one module or 16 modules is the same (5 minutes). Therefore, it would take a minimum of 4 hours (48 modules $\times$ 5 min./module) to find the defects on the 48 failing modules.

Please amend the first full paragraph appearing on page 6 as follows:

The depreciation cost alone on a $1.7 million module tester system is roughly $39 per hour. Thus, the initial module test cost resulting from the equipment alone is $.20 per module. Contrarily, the cost to retest the 48 failures discovered during the initial test is $3.25 per module, a significant increase over the initial test cost. This results in an average module testing cost before rework of $1.02 per module, five times more expensive than without the retesting. It is

thus desirable to have a method of testing memory modules ~~which~~ that avoids the costly retesting of the memory modules.

Please amend the second full paragraph appearing on page 6 as follows:

The present invention addresses the problem of how to avoid the conventional, costly step of retesting memory modules identified as failing during the initial testing of the module by storing the identity of failed module components in a non-volatile memory device such as an EEPROM. Failed module components include such elements as data query ("DQ") terminals and memory bits ~~which~~ that require memory mapping of bad addresses. A plurality of memory dice may be placed on a memory module with other module components and the module ~~than~~ then tested to identify any failed outputs. The locations of failed component parts, such as memory dice, are determinable from the failed output identifiers ~~which~~ that are stored during testing in a non-volatile storage device for access after the testing process. By storing the failed output identities on the memory module itself, locations of specific defective parts may be easily identified and immediately repaired or replaced without the requirement of an additional memory module test, or a requirement of maintaining an association between a particular memory module and its test data. Other module or die information may also be stored on the memory module, such as lot identification numbers or other production information, for access at a later time.

Please amend the first full paragraph appearing on page 7 as follows:

~~Figure~~ FIG. 1 is a front view of a prior art SIMM DRAM assembly;

Please amend the second full paragraph appearing on page 7 as follows:

~~Figure~~ FIG. 2 is a side view of the prior art SIMM DRAM assembly of ~~Fig.~~ FIG. 1;

Please amend the third full paragraph appearing on page 7 as follows:

~~Figure~~ FIG. 3 is a back view of the prior art SIMM DRAM assembly of ~~Fig.~~ FIG. 1;

Please amend the fourth full paragraph appearing on page 7 as follows:

~~Figure~~ FIG. 4 is an illustration of a DIMM DRAM assembly according to the present invention; and

Please amend the fifth full paragraph appearing on page 7 as follows:

~~Figure~~ FIG. 5 is a block diagram of a computer system including non-volatile memory in combination with volatile memory according to the present invention.

Please amend the sixth full paragraph appearing on page 7 as follows:

~~Figure~~ FIG. 4 illustrates a dynamic random access memory ("DRAM") dual in-line memory module ("DIMM") 32. The DIMM 32 shown comprises a printed circuit board ("PCB") 34, or other carrier substrate bearing circuit traces, having a plurality of electrical contacts 36 (numbering 168 in the illustrated example, 84 on each side) along one edge. Each of the electrical contacts 36 is coupled to at least one of a plurality of terminals 37 of functional DRAMs 38, 40, 42, 44, 46, 48, 50 and 52, or an EEPROM 54. The DIMM 32 also includes two impedance resistors 55 and 56 and a temporary connection jumper 57.

Please amend the paragraph bridging pages 7 and 8 as follows:

According to an embodiment of the present invention, a plurality of DRAM dice or chips ~~which~~ that have previously been individually tested and determined to be fully functional, or at least functional to an extent usable within a particular ~~application~~ application, such as a partially good die is included on the DIMM 32. Additionally, more stringent tests may be performed prior to affixation of a given die to a module to establish that a die is also a "known good die" ("KGD"). The functional DRAMs 38, 40, 42, 44, 46, 48, 50 and 52 are then attached, by wire bonding, TAB bonding, flip-chip bonding or other method known in the art, to bond pads (not shown) on the PCB 34 to form the DIMM 32. The DIMM 32 is tested using conventional equipment known in the art such as that previously referenced herein. The identities of any outputs, such as data query ("DQ") terminals, which fail any of the tests in a testing process are detected and recorded in the excess memory of the EEPROM through programming. The

identities of the failed outputs may be recorded either immediately as each fails a test, or at some point subsequent to the test failure, such as at the completion of all tests involving a particular part or at completion of the module test process.

Please amend the second full paragraph appearing on page 8 as follows:

One particular advantage of the present invention is that it may be implemented without costly additional equipment. By modifying the test process software to program the identities of failing outputs into unused portions of the memory in an EEPROM, the advantages of the invention may be achieved. Upon completion of the testing process, any modules ~~which~~ that failed the test may then be placed in an inexpensive apparatus as known in the art where the EEPROM may be read for the identities or locations of terminals and a failure map displayed. From the identities of the failing terminals, the corresponding failing part may be identified and marked for repair or replacement. After repair or replacement, the memory module may again be tested and the process repeated until none of the module parts fail a test.

Please amend the third full paragraph appearing on page 8 as follows:

It is contemplated that the process of the present invention will be particularly beneficial to identifying failed DRAMs, as the failure rate of DRAMs is relatively high. However, as will be clear to one of ordinary skill in the art, the method and apparatus of the present invention may be applied to any testing process where it would be advantageous to have a data record indicative of failed part locations on-board the memory module. It will be understood by those having skill in the technical field of this invention that the invention is applicable to any multi-chip module including a non-volatile storage device including, for example, and without limitation thereto, ~~DRAMs~~ DRAMs, SIMMs, DIMMs and Rambus in-line memory modules ("RIMM")

Please amend the first full paragraph appearing on page 9 as follows:

~~Figure~~ FIG. 5 is a block diagram of a computer system 60 ~~which~~ that includes a memory module 62 tested according to the present invention comprising a plurality of memory devices and at least one non-volatile storage device 63. The computer system 60 includes a processor 64

for performing various computing functions, such as executing specific software to perform specific calculations or tasks. In addition, the computer system 60 includes one or more input devices 68, such as a keyboard or a mouse, coupled to the processor 64 to allow an operator to interface with the computer system 60. Typically, the computer system 60 also includes one or more output devices 70 coupled to the processor 64, such output devices typically being a printer, a video terminal or a network connection. One or more data storage devices 72 are also typically coupled to the processor 64 to store data or retrieve data from external storage media (not shown). Examples of conventional storage devices 72 include hard and floppy disks, tape cassettes, and compact disks. The processor 64 is also typically coupled to a cache memory 74, which is usually static random access memory ("SRAM"), and to the memory module 62.